WEST Search History

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DATE: Monday, April 12, 2004

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		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L30	(current near5 (chang$4 or alter$4 or modif$9 or reduc$4 or lower$4 or less$4)) and (select$4 near3 disabl$4 near3 transistor) and count$4	1
☐	L29	((current near3 amount) near5 (chang$4 or alter$4 or modif$9 or reduc$4 or lower$4 or less$4)) and (select$4 near3 disabl$4 near3 transistor)	3
☐	L28	((current near3 amount) near5 (chang$4 or alter$4 or modif$9 or reduc$4 or lower$4 or less$4)) same (select$4 near3 disabl$4 near3 transistor)	0
☐	L27	l6 and L24	2
☐	L26	l5 and L24	0
☐	L25	l1 and L24	2
☐	L24	l13 or l14 or l15 or l16 or l17 or l18 or l19 or l20 or l21 or l22 or L23	4376
☐	L23	257/e27.001.ccls.	0
☐	L22	257/E27.001.ccls.	0
☐	L21	365/226.ccls.	1811
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☐	L16	320/159.ccls.	44
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☐	L14	713/320.ccls.	510
☐	L13	713/300.ccls.	808
☐	L12	((current near3 amount) near5 (chang$4 or alter$4 or modif$9 or reduc$4 or lower$4 or less$4)) same ((based or depend$4 or respons$4) near5 consum$9)	13
☐	L11	l6.ab.	14
☐	L10	l1.clm.	0
☐	L9	l1.ab.	5
☐	L8	L1 same (reduc$4 or less or lower$4)	11
☐	L7	L6 same (based or depend$4 or respons$4)	8
☐	L6	(gradual$4 near2 reduc$4) with (current near2 amount)	47
☐	L5	(determin$4 or calculat$4) near3 power near3 (need or necessary) near3 (reduc$4 or less) (determin$4 or calculat$4) near3 when near3 power near3 (need or necessary)	29

☐	L4	near3 (reduc$4 or less)	0
☐	L3	L1 same (reduc$4 or less)	10
☐	L2	L1 same (reduc$4 or less or improv$4)	11
☐	L1	(ic or (intergrated adj circuit)) with (current near2 (chang$4 or alter$4 or amount) near3 (rate or speed))	30

END OF SEARCH HISTORY

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End of Result Set

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L29: Entry 3 of 3 File: USPT Nov 14, 2000

DOCUMENT-IDENTIFIER: US 6147513 A
TITLE: Method and circuit for logic input buffer

Abstract Text (1):
A novel logic input buffer having independent DC input trip points (e.g., V.sub.IL and V.sub.IH), reduced cross current during signal transitions, shorter propagation delay, and improved noise performance. The input buffer includes a set of input transistors having dynamically adjustable beta(s) that allows for robust control of the transistor(s) operating characteristics. The beta(s) can be adjusted by changing the size(s) of the input transistors through enabling and disabling selected one(s) of additional input transistor(s).

Brief Summary Text (8):
The present invention provides a novel logic input buffer having one or more of the following benefits: (1) independent DC input trip points (e.g., V.sub.IL and V.sub.IH), (2) reduced cross current during signal transitions, (3) faster switching time, (4) shorter propagation delay, and (5) improved noise performance. The input buffer includes a set of input transistors having dynamically adjustable beta(s) that allows for robust control of the transistor(s) operating characteristics. The beta(s) can be adjusted by changing the size(s) of the input transistors through enabling and disabling selected one(s) of additional input transistor(s).

Detailed Description Text (16):
Second, the output rise time is faster because the P-channel transistors 212 and 216 (size 12/2 in the above example) are sized to pull proportionally less current in the N-channel transistor 214 (size 35/2 in the above example) then the conventional input buffer having a P-channel size of 12/2 and an N-channel size of 70/2. The V.sub.IL level is not affected because the N-channel transistor 214 (size 35/2) is pulling proportionally the same amount of current in the P-channel transistor 212 (size 6/2). However, by decreasing the size of P-channel transistor 212 relative the overall size of the P-channel transistors 212 and 216, faster output rise time can be obtained while reducing the amount of cross current. For example, if transistors 212, 216, and 214 are sized 4/2, 8/2, and 35/2, respectively, the output rise time is faster (12/2 pulling against 35/2) then the conventional input buffer.

Detailed Description Text (30):
A simplified schematic of yet another embodiment of a CMOS inverting input buffer 400 is shown in FIG. 4. The input buffer 400 provides two additional input transistors 416 and 422 that are selectively enabled to provide additional flexibility in the design of the input buffer. Two additional input transistors provide further reduction in the amount of cross current and (possibly) faster switching time than a design utilizing one additional input transistor.

Detailed Description Text (37):
For input buffer 400, since only either transistor 416 or 420 is enabled at any given moment, the cross current is reduced by the transistor that is disabled. For

example, before the falling transition, transistor 416 is disabled and the cross current is limited by transistor 412, even though both N-channel transistors 414 and 420 are enabled. Similarly, before the rising transition, transistor 420 is disabled and the cross current is limited by transistor 414, even though both P-channel transistors 412 and 416 are enabled. Since transistors 412 and 414 are smaller sized than the corresponding transistor 112 and 114, the cross current of input buffer 400 is less than that of input buffer 100 during both rising and falling transitions while still providing independent setting of the V.sub.IH and V.sub.IL trip points. As an example, for a simplified design wherein the sizes of transistor 412 and 416 are each half that of transistor 112 and the sizes of transistors 414 and 422 are each half that of transistor 114, the cross current is reduced by half. The amount of cross current reduces linearly with the transistor size because current is proportional to beta and beta is proportional to transistor size (I .varies..beta., and .beta. .varies. W/L) The sizes of the input transistors 412, 414, 416, and 420 can be selected in the manner described above.

Detailed Description Text (41):
The enable circuit ensures that no (or low leakage) current flows through the input buffer 500 when it is disabled, even if the input is floating or changing. This reduces the amount of current consumption during a standby period and also prevents the input signal from propagating through the input buffer 500 to the output. The enable signal Venb can be couple to the chip enable signal.

L29: Entry 2 of 3 File: USPT Jun 12, 2001

DOCUMENT-IDENTIFIER: US 6246266 B1
TITLE: Dynamic logic circuits using selected transistors connected to absolute voltages and additional selected transistors connected to selectively disabled voltages

Detailed Description Text (20):
Having detailed the effects and benefits of transistors 20.sub.SDVN and 20.sub.SDVP, note that FIG. 2 illustrates these transistors only in connection with a single dynamic logic circuit to simplify the discussion. In a preferred implementation, these devices and their selective disabling operation provided by these transistors is shared with numerous other dynamic logic stages. Indeed, the selective disabling transistors may be used with dynamic logic stages that are out of phase with respect to one another. In any event, using the same selective disabling transistors for different stages provides an efficiency over duplicating such transistors for each stage. For example, based on the different stages coupled to the selectively disabled potential provided by a single selective disabling transistor, an average current that must be supported for all stages can be determined and then the single transistor can be designed with this determination as a consideration. Accordingly, higher and lower demands of individual stages or groups of stages can be averaged into the support provided by a single selectively disabling transistor and without having to customize different an duplicate selectively disabling transistors.

Detailed Description Text (21):
As another inventive aspect of system 16, note that the path from V.sub.DD, to output 18.sub.OUT also includes both a selectively disabling voltage transistor and an LVT transistor that is known to be off in the power down mode. Specifically, this path includes transistor 20.sub.SDVP and p-channel transistor 18.sub.INVP. Transistor 18.sub.INVP is known to be off during the power down mode because that mode is defined to occur when precharge transistor 18.sub.PT is enabled, which thereby disables transistor 18.sub.INVP. Further, since HVT transistor 20.sub.SDVP is disabled during the power down mode, then the voltage at node 18.sub.N3 (i.e., SDV.sub.DD) will begin to float downward from V.sub.DD. Note how this floating voltage affects the LVT transistor known to be off (i.e., transistor 18.sub.INVP). Specifically, the gate potential of transistor 18.sub.INVP during the power down mode is fixed at an absolute voltage, namely, V.sub.DD, and the floating potential at node 18.sub.N3 will then fall as described above. As this floating potential falls, then the V.sub.GS of transistor 18.sub.INVP becomes positive. Here, because transistor 18.sub.INVP is a p-channel transistor, and because it is known in the art that a more positive V.sub.GS as applied to a p-channel transistor reduces the amount of current that the transistor will pass, then the positive V.sub.GS tends to reduced the amount of current that the transistor will leak. Accordingly, the downward floating potential at node 18.sub.N3 in combination with the fixed voltage at the gate of transistor 18.sub.INVP further decreases the tendency of discharge transistor 18.sub.INVP to leak, even though it is an LVT transistor. Also, as the floating potential falls on the order of the approximate difference in the threshold voltages of transistors 20.sub.SDVP and 18.sub.INVP, then the leakage of the LVT transistor 18.sub.INVP is reduced to approximately that of the HVT transistor 20.sub.SDVP and, at that point, the potential at node 18.sub.N3 will reach a stable voltage.

Detailed Description Text (39):
Turning now to additional considerations regarding the threshold voltage of p-channel transistor 20.sub.SDVP, recall from above that when it is driven with an ENABLE signal equal to V.sub.DD +.DELTA.VT, and where .DELTA.VT equals the difference in threshold voltage for an HVT and LVT p-channel transistor, then p-channel transistor 20.sub.SDVP is driven off to an even greater extent than if it were driven only with V.sub.DD. Note further, however, that in some instances there may be a second signal level that is accessible and is greater than V.sub.DD by an amount larger than that described for .DELTA.VT. For example, in many contemporary systems, the I/O voltage levels are larger than the internal supply levels; for example, some current systems use an external I/O voltage level of 3.3 volts and an internal V.sub.DD equal to 1.8 volts. In this or other instances, as an alternative embodiment a voltage larger than V.sub.DD +.DELTA.VT may be used to drive the gate of p-channel transistor 20.sub.SDVP when disabling that transistor and, as a result, the drive voltage would be significantly greater than V.sub.DD +.DELTA.VT voltage where .DELTA.VT equals the difference in threshold voltage for an HVT and LVT transistor. When this even larger drive voltage is used to drive the gate of p-channel transistor 20.sub.SDVP, then its current limiting capability is further increased. In any case, the preceding has provided alternatives for driving p-channel transistor 20.sub.SDVP to further limit its current leakage when it is disabled. As a result, if one of these alternatives is selected, and it is therefore known that p-channel transistor 20.sub.SDVP will provide a sufficient limit on current leakage, then in another embodiment it may well be that its threshold voltage may be reduced so that when it is enabled it provides a larger drive current and thereby increases the speed of system 16. Thus, using one of the many techniques set forth above for producing an LVT transistor, in one embodiment the threshold voltage of p-channel transistor 20.sub.SDVP is adjusted to have a threshold voltage on the order of other p-channel LVT transistors in system 16. Still further, in yet another embodiment the threshold voltage of p-channel transistor 20.sub.SDVP is adjusted to have a threshold voltage lower than that of other p-channel LVT transistors in system 16, such as by making p-channel transistor 20.sub.SDVP a natural transistor or by adjusting its threshold voltage using any one of the various techniques described above for making such an adjustment. Further in this regard, note that if p-channel transistor 20.sub.SDVP is formed as a natural transistor, then it will conduct more current (i.e., have lower resistance) than the other LVT transistors in system 16; as a result, this lower current may used at its full level, or if a lesser amount of current is still usable at a desirable level, then the natural transistor may be made to be a smaller size, thereby driving less current but still providing an enhanced level of current drive relative to an HVT alternative.

L29: Entry 1 of 3 File: USPT Feb 3, 2004

DOCUMENT-IDENTIFIER: US 6686791 B2
TITLE: Oxide anti-fuse structure utilizing high voltage transistors

Brief Summary Text (7):
A more recent fuse structure is the poly fuse ("polysilicon" or "poly resistor" fuse). One advantage of the poly fuse over the metal link fuse is the lesser amount of current required to open the fuse element during programming. However, poly fuses exhibit a pre-burned resistance of 30-100 ohms and a post-burned resistance ranging from a few hundreds to thousands ohms. In addition, poly fuses exhibit a low area density due to a large programming current needed to activate transistors and burn (or blow) the fuse elements after packaged in the IC devices.

CLAIMS:

28. An IC device as claimed in claim 24, wherein the anti-fuse program circuit comprises program units arranged to program one of the anti-fuses, each program unit comprising: a logic gate disposed between a core voltage node and a ground node, and arranged to receive the first and second program voltages, and activate an active "low" state at an output to disable operation of a selected one of the first transistors; and a series of delay elements arranged to receive one of the first and second program voltages, and activate an active "high" state at an output to enable operation of a selected one of the second transistors.

L1: Entry 10 of 30 File: USPT Jul 18, 2000

DOCUMENT-IDENTIFIER: US 6091268 A
TITLE: Potential detecting circuit and semiconductor integrated circuit

Detailed Description Text (7):
Thus, it is possible to determine whether the comparison potential VL reaches the prescribed detection level or not depending on whether the level detection signal GE is H-level or L-level. The detection level is changeable by changing a current conversion rate with which the comparison potential VL is converted into the comparison current IC through changing the resistance value of the variable resistor 2.

Detailed Description Text (11):
Thus, it is possible to determine whether the comparison potential VL reaches the prescribed detection level or not depending on whether the level detection signal GE is H-level or L-level. The detection level is changeable by changing the current conversion rate with which the comparison potential VL is converted into the comparison current IC through changing the resistance value of the variable resistor 2.

Detailed Description Text (20):
The potential detecting circuit of the second preferred embodiment having this configuration, like that of the first preferred embodiment, can determine whether the comparison potential VL reaches the prescribed detection level or not depending on whether the level detection signal GE is H-level or L-level. The detection level for the comparison potential VL is changeable by changing the current conversion rate with which the comparison potential VL is converted into the comparison current IC through changing the resistance value of the variable resistor 2 or by changing the amount of the reference current IR of the variable current source 4.

L27: Entry 1 of 2 File: USPT Dec 29, 1992

DOCUMENT-IDENTIFIER: US 5175485 A
TITLE: Apparatus for controlling charging of a storage battery

Detailed Description Text (36):
As the constant voltage charging continues, as mentioned above, the amount of current flowing to the storage battery 8 is reduced gradually. Then, when the charging of the storage battery 8 is completed and the storage battery 8 begins to be overcharged, the amount of current flowing to the storage battery 8 is again increased because of the presence of a reverse current. For this reason, the voltage at point "K"0 is lower, and thus, the voltage divided through resistors R18 and R19 is also lower.

Current US Original Classification (1):
320/159

L25: Entry 1 of 2 File: USPT Dec 9, 2003

DOCUMENT-IDENTIFIER: US 6661215 B2
TITLE: Semiconductor device with small current consumption having stably operating internal circuitry

Detailed Description Text (40):
In the third embodiment, the returning time T1 of currents I1 and I2 can be set to a desired time period. Therefore, the speed of change of currents I1 and I2 can be set to the highest speed at which power supply potentials VDD1 and VDD2 are not affected by the increase/decrease of I1 and I2, and hence the operation of the non-contact IC card can be made stable and the reliability can be improved.

Current US Cross Reference Classification (3):
365/226

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L11: Entry 4 of 14 File: JPAB Jan 19, 1999

PUB-NO: JP411010152A
DOCUMENT-IDENTIFIER: JP 11010152 A
TITLE: ELECTROLYTIC WATER PREPARATION DEVICE

PUBN-DATE: January 19, 1999

INVENTOR-INFORMATION:
NAME COUNTRY
ACHINAMI, NOBUO

ASSIGNEE-INFORMATION:
NAME COUNTRY
HOSHIZAKI ELECTRIC CO LTD

APPL-NO: JP09161669
APPL-DATE: June 18, 1997

INT-CL (IPC): C02 F 1/46

ABSTRACT:

PROBLEM TO BE SOLVED: To carry out inexpensively the control for keeping the effective chlorine concentration of acid water to be prepared almost constantly by making two of the three settings consisting of the flow rates of water to be electrolyzed, the salt concentration of water to be electrolyzed and the current amount between electrodes almost constant and sequence controlling the remaining one of said settings in compliance with the degree of consumption with time of the electrodes.

SOLUTION: In the case of electrolyzing water to be electrolyzed preparing acid water, voltage is applied between electrodes 15 and 16 in compliance with the state of a flow path changeover valve V. Namely, in the case the flow path changeover valve V is in the positive state, the electrode 15 is used as a positive electrode and the electrode 16 is used as a negative electrode and positive voltage is applied, while in the case the flow path changeover valve V is in the reverse state, the electrode 15 is used as a negative electrode and the electrode 16 is used as a positive electrode and counter voltage is applied. At that time, platinum iridium electrodes are adopted as the electrodes 15 and 16, and the concentration and flow rate of dilute salt water are set almost constant and the sequence control in which the electric current amount between the electrodes 15 and 16 is reduced gradually from the initial set value until the given time is passed in compliance with the degree of consumption with time of the electrodes 15 and 16 and increased gradually toward the initial set value after the given time.

L1: Entry 6 of 30 File: USPT Oct 22, 2002

DOCUMENT-IDENTIFIER: US 6469895 B1
TITLE: Integrated circuit mounting structure including a switching power supply

Brief Summary Text (8):
The length of the power supply conductive paths also aggravates the problem of parasitic inductive reactance between the power supply paths. Due to the high frequency operation of modern ICs, switching power supplies are subject to more and more severe transient loads. The rate of change of current required from a power supply by an IC will, due to the presence of inductance from power supply conductive paths both internal and external to the IC package, result in modulation of the power supply voltage since the current through an inductor cannot change instantaneously. This modulation of the power supply voltage, commonly referred to as power supply noise and voltage sag, can interfere with data transmission on the signal lines or otherwise interfere with IC operation, and thus pose a serious problem to optimum performance of IC circuitry. A common means of controlling the inductance problem is the use of capacitive filters or decoupling capacitors in very close proximity to an IC chip, both between the power supply terminals external to the IC package and within the cavity of the IC package. While such decoupling capacitors are effective in reducing the magnitude of the power supply noise and voltage sag at the IC chip, significant parasitic inductance still remains as a result of the length of the conductive paths between the IC chip and the power supply so that noise and voltage sag still affect the operation of the ICs.

L2: Entry 7 of 11 File: USPT Feb 4, 1997

DOCUMENT-IDENTIFIER: US 5600273 A
TITLE: Constant delay logic circuits and methods

Detailed Description Text (2):
Low Noise Logic (LNL) elements are shown and described in our copending application Ser. No. 08/292,482, filed Aug. 18, 1994. LNL reduces digital noise on the Vss (ground) bus by as much as 66 dB and on the Vdd (+5 Volts) bus by more than 56 dB. The primary technique used by LNL to reduce switching noise is operation with a constant current so that the inductance of the IC distribution, bond wire and package trace would not produce an appreciable voltage due to the product of the inductance and the rate of change of current with respect to time. The logical input to an LNL element does not capacitively couple directly to Vss. LNL complements CMOS logic in specific applications and is intended to be used in combination with CMOS. LNL is especially useful in mixed signal and controlled delay applications and in applications requiring reduced levels of interfering signals radiated or conducted from the partition or the IC.

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L9: Entry 1 of 5 File: JPAB Feb 26, 1999

DOCUMENT-IDENTIFIER: JP 11055936 A
TITLE: DRIVING CIRCUIT FOR INSULATED GATE TRANSISTOR

Abstract Text (2):
SOLUTION: A rate of change in collector current Ic with respect to time dIc/dt of an insulated gate bipolar transistor IGBT1 is feedback-controlled based on the resistance ratios of resistors 26c, 26d for dividing voltage and of resistors 27c, 27d for setting reference voltage, thereby controlling the rate of change in collector current Ic with respect to time within a specified range. By setting the rate of change in collector current Ic with respect of time dIc/dt within a specified range, peak voltage ΔV appearing in the wiring inductance 5 at the time of turn on/turn off of the IGBT1 can be suppressed without using such an element as to have a temperature characteristic like a Zener diode.

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L9: Entry 2 of 5 File: JPAB Jun 25, 1993

DOCUMENT-IDENTIFIER: JP 05161253 A
TITLE: SNUBBER CIRCUIT FOR SEMICONDUCTOR POWER CONVERTER

Abstract Text (2):
CONSTITUTION: A feedback diode 2 is connected in reverse-parallel with a semiconductor switching device 1. An individual RCD charge/discharge type snubber circuit 13 is also connected in parallel with the semiconductor switching device 1. The snubber circuit 13 is composed of a series arm composed of a snubber capacitor 4 and a snubber diode 5 and a discharge resistor am 18 which is connected in parallel with the snubber diode 5. A winding type discharge resistor 17 is employed in the discharge resistor arm 18. The speed of the change of a discharge current Ic created when the switching device 1 is turned on can be suppressed to be a required value by the resistance component R and the inductance component L of the winding type discharge resistor 17. With this constitution, a switching loss can be reduced.

L2: Entry 4 of 11 File: USPT Dec 30, 1997

DOCUMENT-IDENTIFIER: US 5703496 A
TITLE: Method and apparatus for limiting the slew rate of output drivers by selectively programming the threshold voltage of flash cells connected thereto

Brief Summary Text (14):
Because the environment, clock rate, packaging or form factor of an IC may not be known in advance, a system designer must "guess" or otherwise predict what amount of current slew rate reduction is required and design the IC accordingly. The designer must also allow for a sufficient noise margin in the event that the current slew rate reduction is not sufficient. Such can result in an overall IC configured to perform at a clock rate less than would otherwise be desired.

L2: Entry 5 of 11 File: USPT Dec 2, 1997

DOCUMENT-IDENTIFIER: US 5694297 A
TITLE: Integrated circuit mounting structure including a switching power supply

Brief Summary Text (8):
The length of the power supply conductive paths also aggravates the problem of parasitic inductive reactance between the power supply paths. Due to the high frequency operation of modem ICs, switching power supplies are subject to more and more severe transient loads. The rate of change of current required from a power supply by an IC will, due to the presence of inductance from power supply conductive paths both internal and external to the IC package, result in modulation of the power supply voltage since the current through an inductor cannot change instantaneously. This modulation of the power supply voltage, commonly referred to as power supply noise and voltage sag, can interfere with data transmission on the signal lines or otherwise interfere with IC operation, and thus pose a serious problem to optimum performance of IC circuitry. A common means of controlling the inductance problem is the use of capacitive filters or decoupling capacitors in very close proximity to an IC chip, both between the power supply terminals external to the IC package and within the cavity of the IC package. While such decoupling capacitors are effective in reducing the magnitude of the power supply noise and voltage sag at the IC chip, significant parasitic inductance still remains as a result of the length of the conductive paths between the IC chip and the power supply so that noise and voltage sag still affect the operation of the ICs.

L2: Entry 6 of 11 File: USPT Jun 10, 1997

DOCUMENT-IDENTIFIER: US 5638007 A
** See image for Certificate of Correction **
TITLE: Method and apparatus for limiting the slew rate of output drivers of an integrated circuit by using programmable flash cells

Brief Summary Text (14):
Because the environment, clock rate, packaging or form factor of an IC may not be known in advance, a system designer must "guess" or otherwise predict what amount of current slew rate reduction is required and design the IC accordingly. The designer must also allow for a sufficient noise margin in the event that the current slew rate reduction is not sufficient. Such can result in an overall IC configured to perform at a clock rate less than would otherwise be desired.

L7: Entry 5 of 8 File: USPT Oct 11, 1994

DOCUMENT-IDENTIFIER: US 5355336 A
** See image for Certificate of Correction **
TITLE: Memory device and a method for prohibiting writing to the memory device

Detailed Description Text (21):
When a supply voltage is applied to the initial state setting signal generation circuit shown in FIG. 3 after the power is turned on (for example, after battery exchange), the node A obtains a potential substantially identical with the supply voltage, thereby allowing a charging current to flow to the capacitor C for a specified period. The amount of the charging current is gradually reduced until no charging current is allowed to flow after the specified period, whereby the potential of node A nearly becomes zero. When the level of the potential of the node A crosses a threshold voltage V.sub.th of the Schmitt trigger inverter INV at a time t during the specified period, the level of a signal outputted from the Schmitt trigger inverter INV is changed from low to high. Such a low level signal from the Schmitt trigger inverter INV is outputted to the reset input terminal RESET of the second writing restriction register 4. The data stored in the second writing restriction register 4 becomes "0" in response to such a low level signal.

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L7: Entry 7 of 8 File: JPAB Mar 23, 1993

DOCUMENT-IDENTIFIER: JP 05071385 A
TITLE: FUEL INJECTION AMOUNT CONTROL DEVICE FOR DIESEL ENGINE

Abstract Text (2):
CONSTITUTION: An ECTECU 78 is provided for controlling an automatic transmission 65 coupled to a diesel engine 2. An engine ECU 71 to control a fuel injection amount according to the running state of the diesel engine 2 decreases and corrects a fuel injection amount based on communication data from the ECTECU 78 so as to relax a shift shock during a shift. The engine ECU 71 performs moderating control through gradual regulation and correction of a fuel injection amount during acceleration and deceleration of the diesel engine 2. Further, the engine ECU 71 prohibits moderating correction of an injection amount during a shift so as to decrease and correct the injection amount. Though an injection amount to the diesel engine 2 is decreased for correction during a shift, this constitution immediately reduces a current injection amount instead of gradual reduction of it.

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L2: Entry 1 of 11 File: USPT Dec 9, 2003

DOCUMENT-IDENTIFIER: US 6661215 B2
TITLE: Semiconductor device with small current consumption having stably operating internal circuitry

Detailed Description Text (40):
In the third embodiment, the returning time T1 of currents I1 and I2 can be set to a desired time period. Therefore, the speed of change of currents I1 and I2 can be set to the highest speed at which power supply potentials VDD1 and VDD2 are not affected by the increase/decrease of I1 and I2, and hence the operation of the non-contact IC card can be made stable and the reliability can be improved.

L2: Entry 2 of 11 File: USPT Oct 22, 2002

DOCUMENT-IDENTIFIER: US 6469895 B1
TITLE: Integrated circuit mounting structure including a switching power supply

Brief Summary Text (8):
The length of the power supply conductive paths also aggravates the problem of parasitic inductive reactance between the power supply paths. Due to the high frequency operation of modern ICs, switching power supplies are subject to more and more severe transient loads. The rate of change of current required from a power supply by an IC will, due to the presence of inductance from power supply conductive paths both internal and external to the IC package, result in modulation of the power supply voltage since the current through an inductor cannot change instantaneously. This modulation of the power supply voltage, commonly referred to as power supply noise and voltage sag, can interfere with data transmission on the signal lines or otherwise interfere with IC operation, and thus pose a serious problem to optimum performance of IC circuitry. A common means of controlling the inductance problem is the use of capacitive filters or decoupling capacitors in very close proximity to an IC chip, both between the power supply terminals external to the IC package and within the cavity of the IC package. While such decoupling capacitors are effective in reducing the magnitude of the power supply noise and voltage sag at the IC chip, significant parasitic inductance still remains as a result of the length of the conductive paths between the IC chip and the power supply so that noise and voltage sag still affect the operation of the ICs.

L7: Entry 1 of 8 File: USPT Nov 18, 2003

DOCUMENT-IDENTIFIER: US 6650354 B2
TITLE: Image recorder having diagnostic capability

Detailed Description Text (38):
The following is why the amount of current supplied to the laser light source 21 is gradually reduced to slowly turn off the laser light source 21. When a semiconductor laser is used as the laser light source 21, a sudden change in the amount of current, depending on the amount of current supplied to the laser light source 21 and electric wiring conditions, may produce a surge current and cause damage on the laser light source 21. For this reason, the image recorder according to this preferred embodiment is configured such that the light shielding mechanism 22 prevents the application of a laser beam to the recording medium 11 or the like and then the amount of current supplied to the laser light source 21 is gradually reduced to slowly turn off the laser light source 21.

L7: Entry 3 of 8 File: USPT Jun 8, 1999

DOCUMENT-IDENTIFIER: US 5910861 A
TITLE: Technique for controlling the write currents of a magnetic disk recording apparatus

Brief Summary Text (14):
According to one aspect of the present invention, a circuit for controlling the write currents of a magnetic disk recording apparatus comprises a read/write circuit for performing a write or read operation according to the read/write mode signal and for supplying a constant write current to a magnetic head in response to a write data in the write mode, a write current adjustment means connected to the read/write circuit for adjusting step by step the amount of the write current supplied to the head under a given control, a timing control circuit for prolonging the read mode of the read/write circuit for a predetermined time on a transit of the mode signal state from the write to the read mode, and a micro controller for controlling the write current adjustment to gradually reduce the amount of the write current for a given time in response to the end of a write gate signal defining write intervals in the write mode.

CLAIMS:

1. A circuit for controlling the write currents of a magnetic disk recording apparatus comprising:

a read/write circuit for performing a write or read operation according to a read/write mode signal and for applying a constant write current to a magnetic head in response to a write data in the write mode;

a write current adjustment circuit connected to said read/write circuit for adjusting step by step the amount of the write current applied to the head under a given control, the write current adjustment circuit comprising a pulse width modulation (PWM) signal generator having an input and an output, and further comprising first and second field effect transistors (FETs) and first and second and third resistors and a capacitor; the output of the PWM signal generator being connected to a gate of the first FET and a source of the first FET being grounded and a drain of said first FET being connected to one end of the first resistor, the other end of the first resistor being connected to a junction point of one end of the capacitor and one end of the second resistor, the other end of the second resistor being connected to the read/write circuit, the other end of the capacitor being grounded, a drain of the second FET being grounded and a source of the second FET being connected to one end of the third resistor, the other end of the third resistor being connected to the read/write circuit;

a timing control circuit for prolonging the read mode of said read/write circuit for a predetermined time on a transit of the mode signal state from the write to the read mode, the timing control circuit having one output being connected to a gate of the second FET via an inverter; and

a micro controller for controlling said write current adjustment circuit to gradually reduce the amount of the write current for a given time in response to the end of a write gate signal defining write intervals in the write mode, the

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Detailed Description Text (4):
Further, the data output buffer comprises a delay circuit 24 and a second NOR gate 26 for commonly receiving the inverted data signal from the first node 17, and a second PMOS transistor M2 connected between the supply voltage source Vcc and the output line 15. The delay circuit 24 delays the inverted data signal from the first node 17 for a predetermined time period and supplies the resultant logic signal as shown in FIG. 2D to the second NOR gate 26. The second NOR gate 26 perform a NOR function on the output signal from the delay circuit 24 and the inverted data signal from the first node 17 and generates the resultant pulse signal which has a high logic pulse width corresponding to the delay time of the delay circuit 24. The pulse signal from the second NOR gate 26 is applied to an inverter 28. The inverter 28 inverts the pulse signal from the second NOR gate 26 and outputs the inverted pulse signal as shown in FIG. 2F to a gate of the second PMOS transistor M2. The second PMOS transistor M2 is turned on for a short duration of the inverted pulse signal from the inverter 28. Consequently, the second PMOS transistor M2 transfers the supply voltage from the supply voltage source Vcc to the output line 15 through its source and drain. As a result, the second PMOS transistor M2 is turned on for the delay time of the delay circuit 24 from the moment that the first PMOS transistor M1 is turned on, to increase an amount of current being supplied to the output line 15. The second PMOS transistor M2 has a channel width wider than that of the first PMOS transistor M1 to transfer a larger amount of current than that of the first PMOS transistor M1. For this reason, as shown in FIG. 2G, a voltage on the output line 15 is initially increased abruptly due to the current amount flowing thereto through the first and second PMOS transistors M1 and M2 and then gradually reduced to a desired level because of the supply of no current through the second PMOS transistor M2. Then, the voltage on the output line 15 remains at the desired level. As a result, an output signal generated on the output line 15 has an enhanced response speed with respect to the data signal. The first PMOS transistor M1 functions as a main pull-up driver, whereas the second PMOS transistor M2 functions as an auxiliary pull-up driver. The inverter series circuit 16 and 18 delays the inverted data signal from the first node 17 by propagation delay times of the delay circuit 24, the second NOR gate 26 and the inverter 28 so that the first and second PMOS transistors M1 and M2 can simultaneously be driven.

Detailed Description Text (9):
Further, the data output buffer comprises a second PMOS transistor M2 connected between the supply voltage source Vcc and the output line 35, a comparator 44 for inputting a reference voltage V.sub.OH from a second input line 41, and a second NMOS transistor M4 connected between an output terminal of the comparator 44 and the ground voltage source Vss. The comparator 44 also has a control terminal for inputting the inverted data signal from the first node 37. When the inverted data signal from the first node 37 is low in logic, the comparator 44 compares a voltage of an output signal on the output line 35 with the reference voltage V.sub.OH from the second input line 41. If the voltage of the output signal on the output line 35 is lower than the reference voltage V.sub.OH from the second input line 41, the comparator 44 generates a high logic comparison signal. On the contrary, if the voltage of the output signal on the output line 35 is higher than the reference

voltage V.sub.OH from the second input line 41, the comparator 44 generates a low logic comparison signal. As a result, the comparator 44 generates a pulse signal which has a high logic pulse width corresponding to a time period from a falling edge of the inverted data signal from the first node 37 until the voltage of the output signal on the output line 35 reaches the reference voltage V.sub.OH. The pulse signal from the comparator 44 is applied to an inverter 46. The inverter 46 inverts the pulse signal from the comparator 44 and outputs the inverted pulse signal as shown in FIG. 4F to a gate of the second PMOS transistor M2. The second PMOS transistor M2 is turned on for a short duration of the inverted pulse signal from the inverter 46. Consequently, the second PMOS transistor M2 transfers the supply voltage from the supply voltage source Vcc to the output line 35 through its source and drain. As a result, the second PMOS transistor M2 is turned on for a time period from the turning-on of the first PMOS transistor M1 until the voltage of the output signal on the output line 35 arrives at the reference voltage V.sub.OH, to increase an amount of current being supplied to the output line 35. The second PMOS transistor M2 has a channel width wider than that of the first PMOS transistor M1 to transfer a larger amount of current than that of the first PMOS transistor M1. For this reason, as shown in FIG. 4G, a voltage on the output line 35 is initially increased abruptly above the reference voltage V.sub.OH due to the current amount flowing thereto through the first and second PMOS transistors M1 and M2 and then gradually reduced to the reference voltage V.sub.OH because of the supply of no current through the second PMOS transistor M2. Then, the output signal on the output line 35 remains stably at the reference voltage V.sub.OH. In result, the output signal on the output line 35 has an enhanced response speed with respect to the data signal. The first PMOS transistor M1 functions as a main pull-up driver, whereas the second PMOS transistor M2 functions as an auxiliary pull-up driver. The inverter series circuit 36 and 38 delays the inverted data signal from the first node 37 by propagation delay times of the comparator 44 and the inverter 46 so that the first and second PMOS transistors M1 and M2 can simultaneously be driven. Also, the inverter series circuit 40 and 42 acts to apply the inverted and delayed data signal to the gate of the first NMOS transistor M3 at the same time that the logic signal from the inverter series circuit 36 and 38 is applied to the gate of the first PMOS transistor M1. On the other hand, the inverted data signal from the first node 37 is also applied to a gate of the second NMOS transistor M4. When the inverted data signal from the first node 37 is high in logic, the second NMOS transistor M4 is turned on, so as to transfer the ground voltage from the ground voltage source Vss to an input terminal of the inverter 46 through its source and drain. In result, the second NMOS transistor M4 acts to prevent a faulty operation of the inverter 46 when the output signal from the comparator 44 is at a high impedance state.